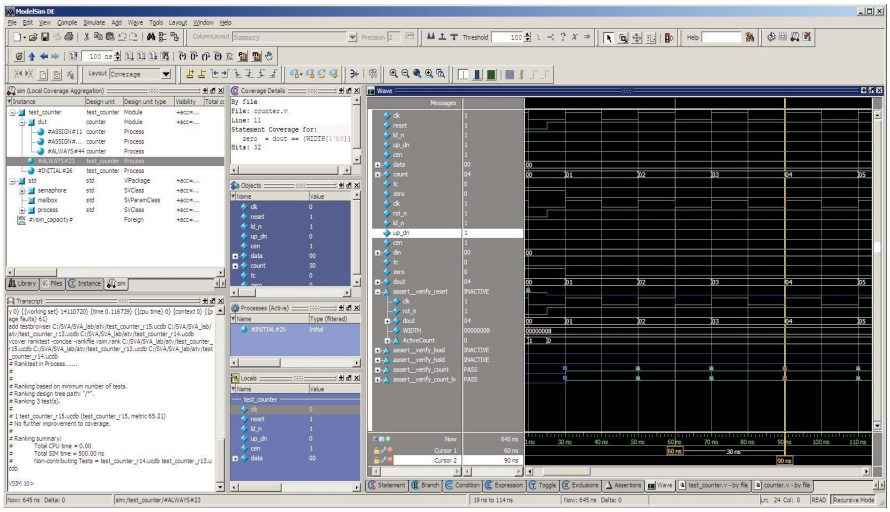
HDL Simulation
ModelSim DE



ModelSim DE offers the most verification capabilities in its class, including assertion-based verification.

Sophisticated FPGA Verification

ModelSim® DE packs an unprecedented level of verification capabilities in a cost-effective HDL simulation solution. In addition to supporting standard HDLs, ModelSim DE increases design quality and debug productivity.

ModelSim's award-winning Single Kernel Simulator (SKS) technology enables transparent mixing of VHDL and Verilog in one design. Its architecture allows platform-independent compile with the outstanding performance of native compiled code. The graphical user interface is powerful, consistent, and intuitive. All windows update automatically following activity in any other window. For example, selecting a design region in the Structure window automatically updates the Source, Signals, Process, and Variables windows. You can edit, recompile, and re-simulate without leaving the ModelSim environment. All user interface operations can be scripted and simulations can run in batch or interactive modes.

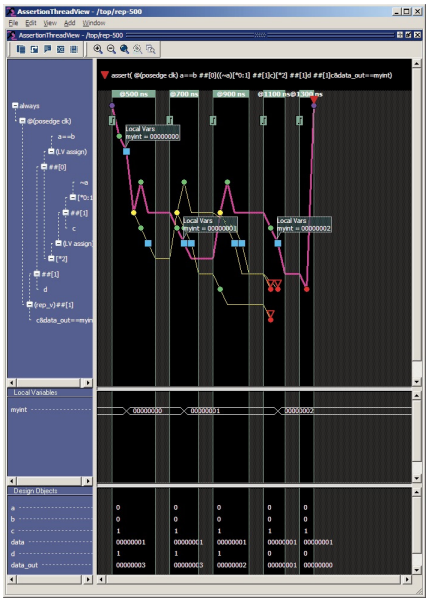
ModelSim DE simulates behavioral, RTL, and gate-level code, including VHDL VITAL and Verilog gate libraries, with timing provided by the Standard Delay Format (SDF).

Assertion-Based Verification with SVA and PSL

Assertion-based verification (ABV) improves design quality through the insertion of white-box monitors that provide a window allowing active monitoring of functional correctness. Assertions catch errors that tests activate but fail to propagate to typical black-box observation points; such as the primary outputs. The assertions also turbocharge time-to-debug productivity because they identify functional bugs much closer to the

FEATURES AND BENEFITS:

- Native compiled, Single Kernel Simulator technology
- VHDL, Verilog, PSL, and SystemVerilog design and assertions constructs
- Intelligent, easy-to-use GUI with Tcl interface
- Integrated project management, source code templates, and wizards
- Wave viewing and comparison; objects, watch, and memory windows increase debug productivity
- Code coverage
- Standard support for Xilinx SecureIP
- SystemC option available



The Assertion Thread Viewer shows a complete assertion evaluation identifying why each thread passes or fails.

root cause. The time savings from a significantly shorter causality traceback can reach hours or even days.

ModelSim DE enables ABV through support of SystemVerilog Assertion (SVA) constructs and the Property Specification Language (PSL). Both SVA and PSL assertions can be either embedded within the design HDL source code or specified in separate units, then bound to the appropriate module instance in the design hierarchy.

Assertion Thread Viewer and Assertion Browser

When complex assertions are triggered, it can be challenging to determine the cause of the failure by examining simulation results in only the Wave window. Assertions can be logged to the Wave window where activation, success, and failure states are easily identified. Since assertions can have multiple threads in concurrent evaluation, ModelSim DE includes an innovative Assertion Thread Viewer, which graphically shows the complete evaluation of an activated assertion. Each thread in the evaluation is displayed, as is the successor failure of every Boolean expression evaluated in the sequence of each thread. Local variable values are also displayed for a complete assertion debug environment. Statistics for each assertion can be examined in the Assertion Browser window. Assertion statistics include the number of activations, successes, failures, and vacuous successes for each assertion.

A More Intelligent GUI

An intelligently engineered GUI makes efficient use of desktop real estate. ModelSim DE offers a highly intuitive arrangement of interactive graphical elements (windows, toolbars, menus, etc.), making it easy to view and access the many powerful capabilities of ModelSim. The result is a feature-rich GUI that is easy to use and quickly mastered. ModelSim redefined openness in simulation by incorporating the Tcl user interface into its HDL simulator. Tcl is a simple but powerful scripting language for controlling and extending applications.

The ModelSim DE GUI delivers highly productive design debug and analysis capabilities as well as project and file management.

Memory Window

The memory window allows intuitive and flexible viewing and debugging of design memories.

VHDL and Verilog memories are auto-extracted from the source and viewed in the GUI, allowing powerful search, fill, edit, load, and save functionality. The Memory window supports pre-loading memories from a file or using constant, random, and computed values, saving the time-consuming step of initializing sections of testbenches just to load memories. All functions are available via the command line, allowing their use in scripting.

Waveform and Results Viewing

ModelSim DE provides a high performance, full-featured Wave window. The Wave window provides cursors for marking interesting points in time and measuring the time distance between cursors. Wave window contents can be formatted flexibly through powerful virtual signal definitions and grouping.

Waveform comparisons are easily performed between two simulation results. Timing differences between RTL and gate-level simulation results are easily handled through user-specified time-filtering capabilities.

ModelSim provides a unique WFL management utility (aka WLFMAN) that allows the manipulation of wlf result files, enabling you to specify the amount of information to record to a WLF file or to subset an existing WLF file based on signals or time. The WLFMAN utility allows efficient management of disk space and post-simulation debug efficiency.

Source Window Templates and Wizards

VHDL and Verilog templates and wizards allow you to quickly develop HDL code without having to remember the exact language syntax. All the language constructs are available with a click of a mouse. Easy-to-use wizards step

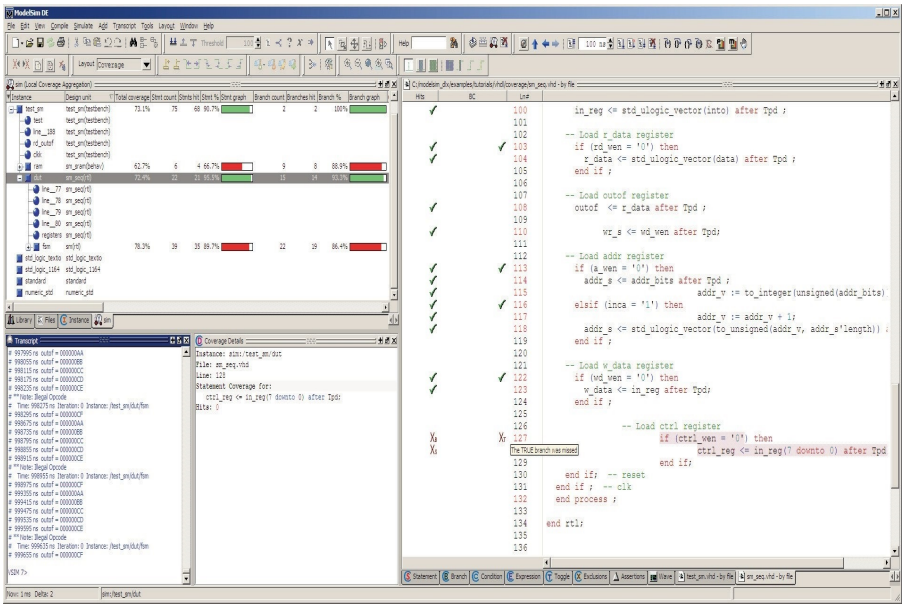
you through creation of more complex HDL blocks. The wizards show how to create parameterizable logic blocks, testbench stimuli, and design objects. The source window templates and wizards benefit both novice and advanced HDL developers with time-saving shortcuts.

Project Manager

The Project Manager greatly reduces the time it takes to organize files and libraries. As you compile and simulate, the Project Manager stores the unique settings of each individual project, allowing you to restart the simulator right where you left off. Simulation properties allow you to easily re-simulate with pre-configured parameters.

Code Coverage

Design verification completeness can be measured through code coverage. ModelSim DE supports statement, expression, condition, toggle, and FSM coverage. Code coverage metrics are automatically derived from the HDL source. As many design blocks are created to be configurable and reusable and not all metrics are valuable, code coverage metrics can be flexibly managed with source code pragmas and exclusions specified in the code coverage browser.



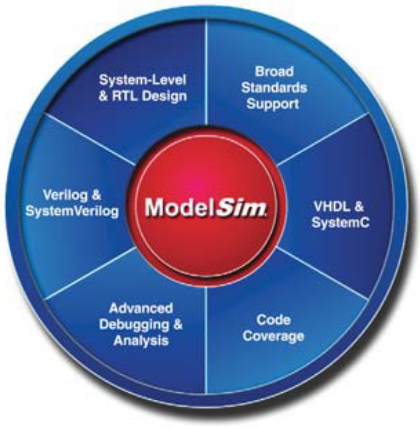
Using integrated code coverage, ModelSim DE tracks how much of the design has been tested.

A Powerful, Cost-Effective Simulation Solution

ModelSim DE delivers a powerful simulation solution ideally suited for the verification of small and medium sized FPGA designs; especially designs with complex, mission critical functionality.

Platform Support

ModelSim DE is supported on the 32/64-bit Windows 7, 8.1, 10 and Linux RHEL 6-, 7- and SLES 11-based platforms.



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