

Rapid

Design for Reliability

Automated Electrical Stress Analysis for Design Engineers

- ✓ Performs rapid Electrical Stress Analysis (ESA) and derating based on DC worst-case scenarios
- ✓ Detects electrical stress errors during schematic design
- ✓ Detects design errors that are caused by insufficient power supply voltage or current
- ✓ Detects design and Net-name conflicts
- ✓ Provides accurate Mean Time Between Failure (MTBF) and Service Life Results

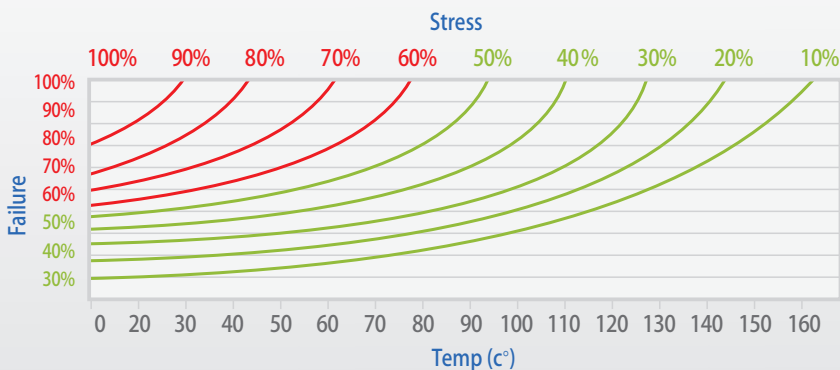
fiXtress Rapid replaces the manual stress calculations performed by design engineers during the design process with an intelligent, interactive, quick and automated process.

Automated Stress Analysis enables engineers to:

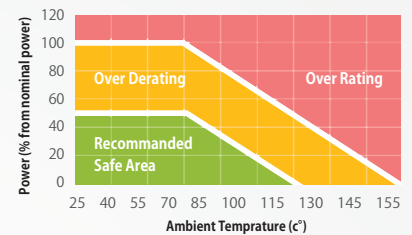
- ✓ Easily select components based on appropriate derating levels
- ✓ Identify voltage-level conflicts in IC and Net-name pins
- ✓ Implement standard Net-naming guidelines
- ✓ Take advantage of preliminary thermal placement suggestions
- ✓ Ensure that each IC power supply input complies with its manufacturer's specifications

fiXtress Rapid can analyze an incomplete design, enabling multiple engineers to work concurrently on the same design. Analysis can therefore be performed before the final BOM freeze.

fiXtress Rapid identifies problems early in the design process when they are easier and most cost-effective to fix.



Increased stress, even at low temperatures, results in 100% failure



BENEFITS

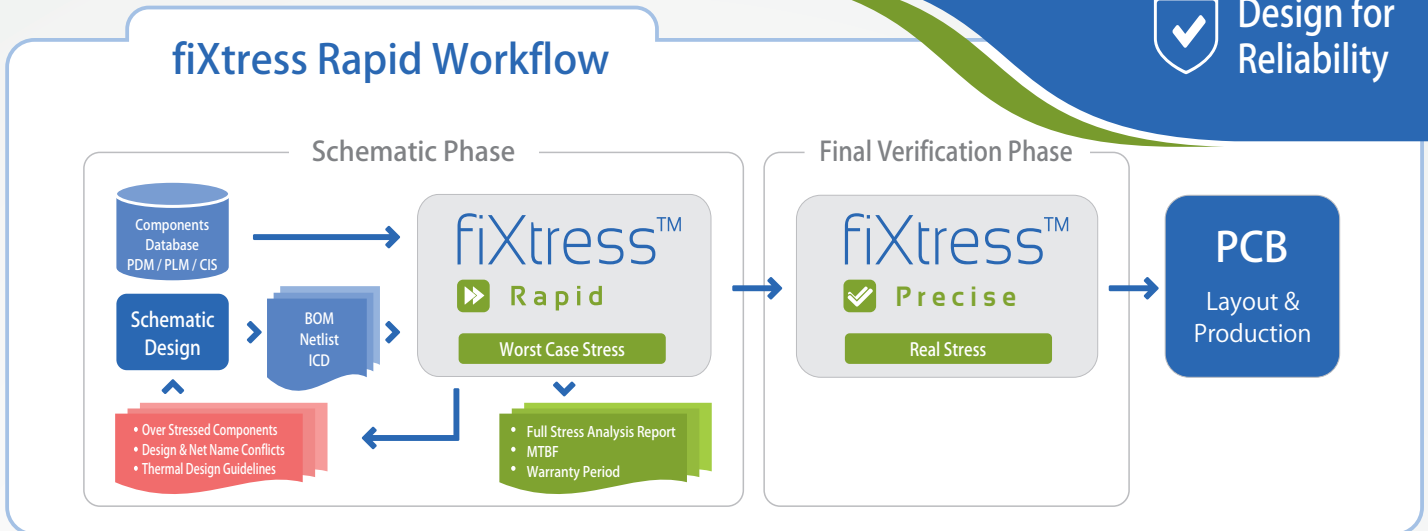
- Accelerates time to market by reducing design cycles
- Optimizes component rating/size selection
- Improves system reliability & MTBF
- Complements fiXtress Schematic Review results by checking power and voltage budgets
- Optimizes thermal design placement

FEATURES

- Fast, automated stress analysis
- Calculates stress levels based on DC worst-case scenarios
- Enables selection of component rating based on appropriate derating guidelines
- Implements standard Net-naming guidelines
- Identifies voltage-level conflicts in IC and Net-names
- Provides preliminary thermal placement guidance
- Analyzes designs even when they are incomplete
- Can be quickly repeated after each design modification



Rapid



Reducing EOS with Stress Analysis

Electrical Over Stress (EOS) is a key failure factor in electronics. Using fiXtress Rapid, design engineers can quickly identify over-stressed components and easily determine the root cause of the problem, such as design conflicts or rating errors.

Early detection of EOS issues dramatically reduces design time, design cycles and component failure in PCB prototype testing.

Data Import

fiXtress Rapid imports:

- ✓ **Netlist and BOM:** The current design's Netlist and BOM for each design iteration.
- ✓ **ICD:** The Inter-Connect Document (ICD), which defines the power supply source input and circuit loads. (Optional)

fiXtress Rapid Analysis

The schematic design represented by the BOM and Netlist is used to calculate the electrical stress of the components. These calculations use data from the Components Database, which represents the datasheet's parameters.

This data is used to calculate operational parameters, such as power dissipation, voltage, current and junction temperature. These calculations use ICD data for power input constraints.

During this analysis process, fiXtress Rapid also identifies design and Net-name conflicts.

fiXtress Rapid then checks whether the components' stress values meet the derating criteria, based on worst-case scenarios.

Output

fiXtress Rapid's analysis provides design engineers with the following output results:

- ✓ Over-stressed components
- ✓ Identified design and Net-name conflicts
- ✓ Over-designed components
- ✓ Thermal placement guidelines in the form of a Pareto list, starting with the components that have the highest temperature, for optimal placement during layout

fiXtress Rapid is the next-generation EDA tool for improving PCB reliability and robustness.